REMARKS

This paper is responsive to a Final Office action dated September 26, 2006. Claims 1-46 were examined. Claims 20-46 have been withdrawn from consideration in response to the Examiner's Restriction Requirement.

Claim Rejections Under 35 USC § 103(a)

Claims 11-15 and 18-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U. S. Patent No. 6,463,570 B1 to Dunn et al. (hereinafter, "Dunn"). Claims 16 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dunn in view of U. S. Patent No. 5,943,488 to Raza (hereinafter, "Raza").

Regarding claim 1, Applicant respectfully maintains that the Office has failed to establish a *prima facie* case of obviousness. In particular, Dunn, alone or in combination with other references of record, fails to teach or suggest

> a first capacitive load for characterizing at least one layer of an interconnect structure in the integrated circuit, the first capacitive load being selectively coupled to the speed sensing circuit, the first capacitive load being formed by at least a portion of a first metal trace residing in a first metal layer and at least a portion of a second metal trace residing in a second metal layer, the first and second metal layers being separated by at least an insulating layer,

as required by claim 1. The Office action admits that Dunn fails to teach a first capacitive load being selectively coupled to a speed sensing circuit, as claimed. The Office action fails to provide a reference that teaches or suggests that a first capacitive load is selectively coupled with the speed sensing circuit. Rather, the Office action merely states that using a selection process to characterize individual interconnect layers would enhance the characterization process of the layered interconnections and therefore, the Office concludes that it would be obvious to modify

the teachings of Dunn in order to obtain the invention of claim 1. Thus, the Office action introduces hindsight into the obviousness analysis. Applicant respectfully points out that "'[d]efining the problem in terms of its solution reveals improper hindsight in the selection of prior art relevant to obviousness.'" See Ecolochem Inc. v. S. Cal. Edison, 56 USPQ2d 1065, 1073 (Fed. Cir. 2000) (citations omitted). Indeed, "'obvious to try' is not the standard." See Ecolochem, 56 USPQ2d at 1075.

In addition, Applicant respectfully maintains that Dunn teaches away from a first capacitive load for characterizing at least one layer of an interconnect structure in the integrated circuit, the first capacitive load being selectively coupled to the speed sensing circuit, the first capacitive load being formed by at least a portion of a first metal trace residing in a first metal layer and at least a portion of a second metal trace residing in a second metal layer, the first and second metal layers being separated by at least an insulating layer, as required by claim 1. Dunn teaches that the "structure of the inverters constituting each ring oscillator is implemented in accordance with a predetermined set of parameters which are selected to sensitize the ring oscillator to variations in the fabrication process steps being verified." Col. 5, lines 55-59. Applicant points out that "'[a] reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference or would be led in a direction divergent from the path that was taken by the applicant.'" In re Kahn, 441 F.3d 977, 990, 78 U.S.P.Q.2d (BNA) 1329, 1338 (Fed. Cir. 2006) (citations omitted) (emphasis added). Since Dunn teaches sensitizing a ring oscillator to process steps of interest by implementing particular design features of the ring oscillator stages, (col. 5, lines 10-49) Dunn teaches away from selectively coupling a capacitive load to a speed sensing circuit, as required by claim 1.

Since Dunn does not disclose or suggest the recited limitation and no other art of record adds the missing disclosure, Applicant respectfully requests that the rejection of claim 1 and all claims dependent thereon, be withdrawn.

Regarding claim 18, Applicant respectfully maintains that the Office has failed to establish a *prima facie* case of obviousness. In particular, Dunn, alone or in combination with other references of record, fails to teach or suggest

> a first capacitive load for characterizing at least one layer of an interconnect structure in the integrated circuit, the first capacitive load being selectively coupled to the speed sensing circuit, the first capacitive load being formed by at least a portion of a first metal trace residing in a first metal layer and at least a portion of a second metal trace residing in a second metal layer, the first and second metal layers being nonadjacent metal layers,

as required by claim 18. The Office action admits that Dunn fails to teach a first capacitive load being selectively coupled to a speed sensing circuit, as claimed. The Office action fails to provide a reference that teaches or suggests that a first capacitive load is selectively coupled with the speed sensing circuit. Rather, the Office action merely states that using a selection process to characterize individual interconnect layers would enhance the characterization process of the layered interconnections and therefore, the Office concludes that it would be obvious to modify the teachings of Dunn in order to obtain the invention of claim 18. Thus, the Office action introduces hindsight into the obviousness analysis. Applicant respectfully points out that "'[d]efining the problem in terms of its solution reveals improper hindsight in the selection of prior art relevant to obviousness.'" See Ecolochem Inc. v. S. Cal. Edison, 56 USPQ2d 1065, 1073 (Fed. Cir. 2000) (citations omitted). Indeed, "'obvious to try' is not the standard." See Ecolochem, 56 USPQ2d at 1075.

In addition, Applicant respectfully maintains that Dunn teaches away from a first capacitive load for characterizing at least one layer of an interconnect structure in the integrated circuit, the first capacitive load being selectively coupled to the speed sensing circuit, the first capacitive load being formed by at least a portion of a first metal trace residing in a first metal layer and at least a portion of a second metal trace residing in a second metal layer, the first and second metal layers being nonadjacent metal layers, as required by claim 18. Dunn teaches that the "structure of the inverters constituting each ring oscillator is implemented in accordance with a predetermined set of parameters which are selected to sensitize the ring oscillator to variations in the fabrication process steps being verified." Col. 5, lines 55-59. Applicant points out that

"'[a] reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference or would be led in a direction divergent from the path that was taken by the applicant.'" In re Kahn, 441 F.3d 977, 990, 78 U.S.P.Q.2d (BNA) 1329, 1338 (Fed. Cir. 2006) (citations omitted) (emphasis added). Since Dunn teaches sensitizing a ring oscillator to process steps of interest by implementing particular design features of the ring oscillator stages, (col. 5, lines 10-49) Dunn teaches away from selectively coupling a capacitive load to a speed sensing circuit, as required by claim 18.

Since Dunn does not disclose or suggest the recited limitation and no other art of record adds the missing disclosure, Applicant respectfully requests that the rejection of claim 18 and all claims dependent thereon, be withdrawn.

Claims 16 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dunn in view of U. S. Patent No. 5,943,488 to Raza. Applicant believes that claims 16 and 17 depend from allowable base claims and are allowable for at least this reason.

In summary, all claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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